Title: EFFICIENT VERIFICATION FOR COURSE/FINE PROGRAMMING OF NON-VOLATILE MEMORY
Applicants: Guterman, et al. Docket No.: SAND-01011US0
Appl. No.: Unknown Atty: Burt Magen
Filing Date: January 27, 2004 Phone: (415) 369-9660
Express Mail No.: EV 391 867 388 US

Fig. 1

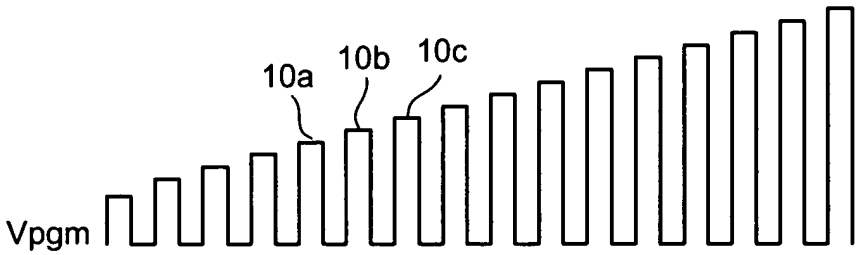
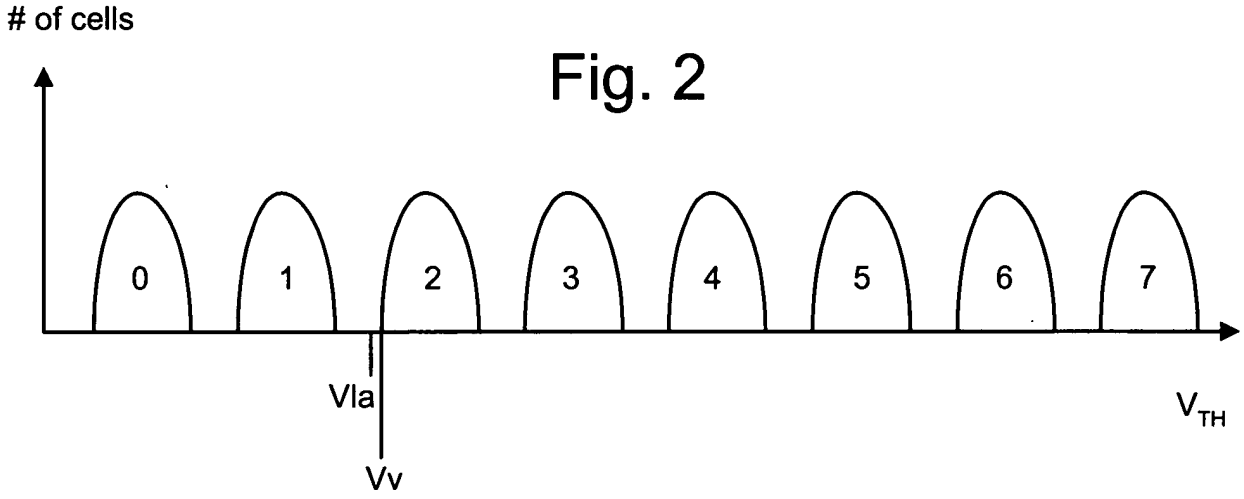


Fig. 2



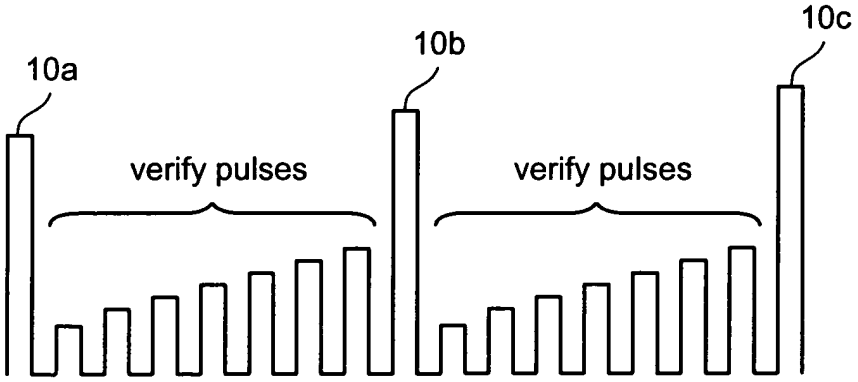


Fig. 3

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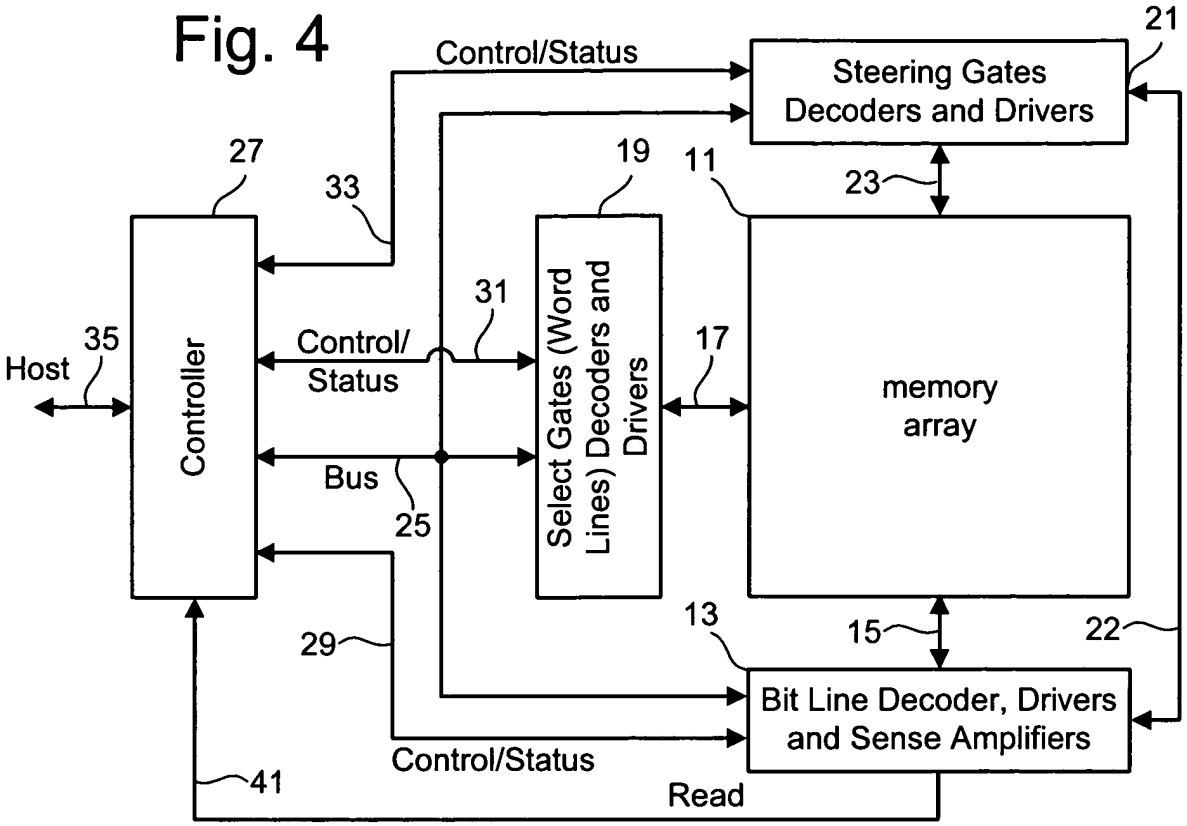
Fig. 4



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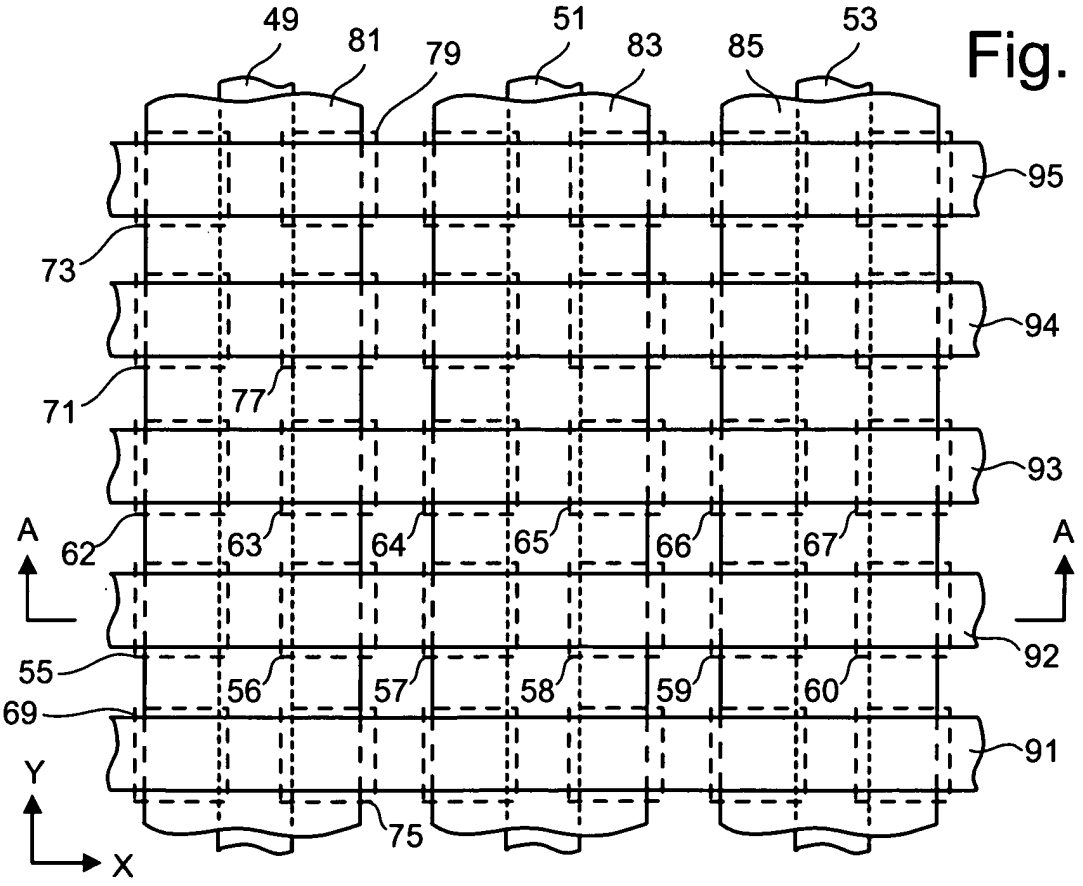

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Fig. 6

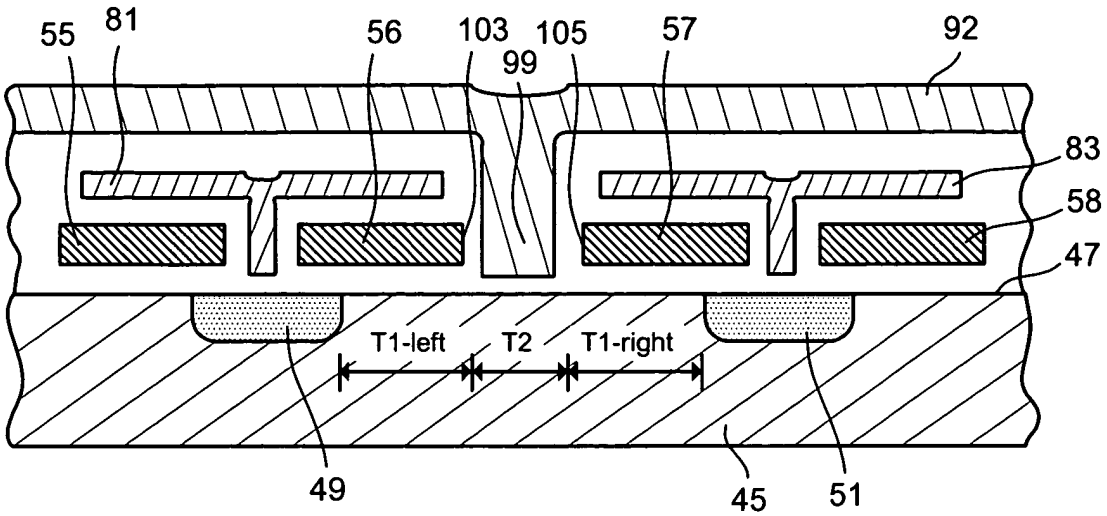

Fig. 7

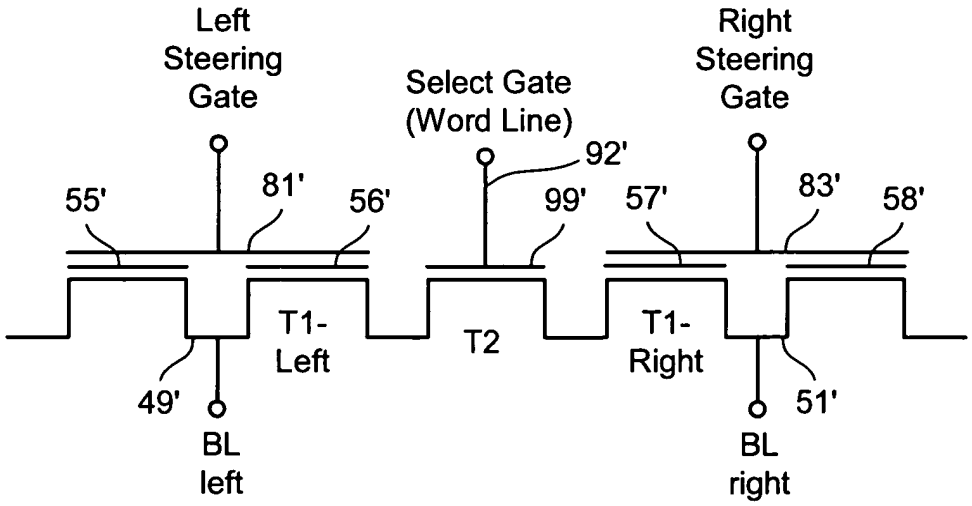

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Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW	0	X	X	X	X
(2) ERASE (TO WORD LINE)	V_E	5	0	0	5
(3) READ LEFT FLOATING GATE	V_{SR}	0	V_M	V_{BR}	1
(4) READ RIGHT FLOATING GATE	V_{SR}	1	V_{BR}	V_M	0
(5) PROGRAM LEFT FLOATING GATE	V_{SP}	5	V_P	V_{BP}	0
(6) PROGRAM RIGHT FLOATING GATE	V_{SP}	0	V_{BP}	V_P	5
(7) NO PROGRAM IN SELECTED ROW	V_{SP}	0 5	X X	X X	0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO V_E, AND THE SUBSTRATE AT ZERO VOLTS]	V_{SE}	FLOAT	0	0	FLOAT

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Fig. 9A

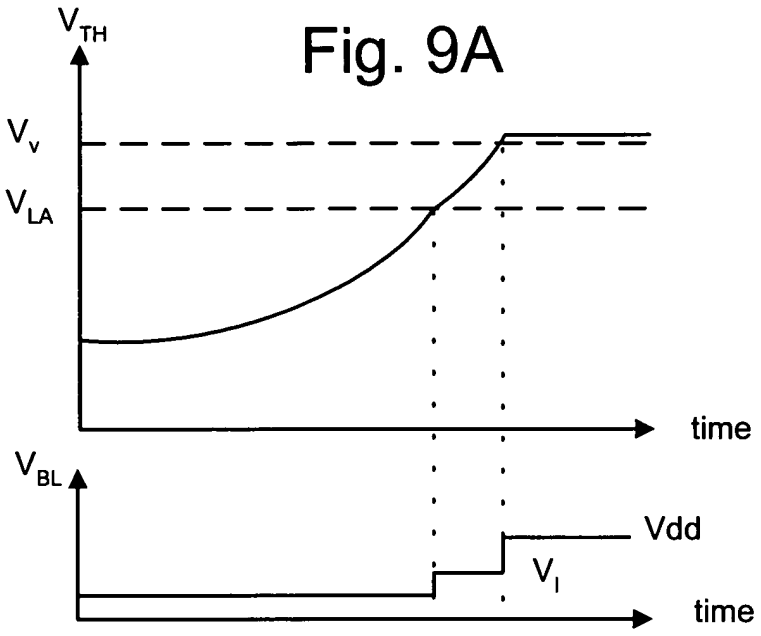

Fig. 9B

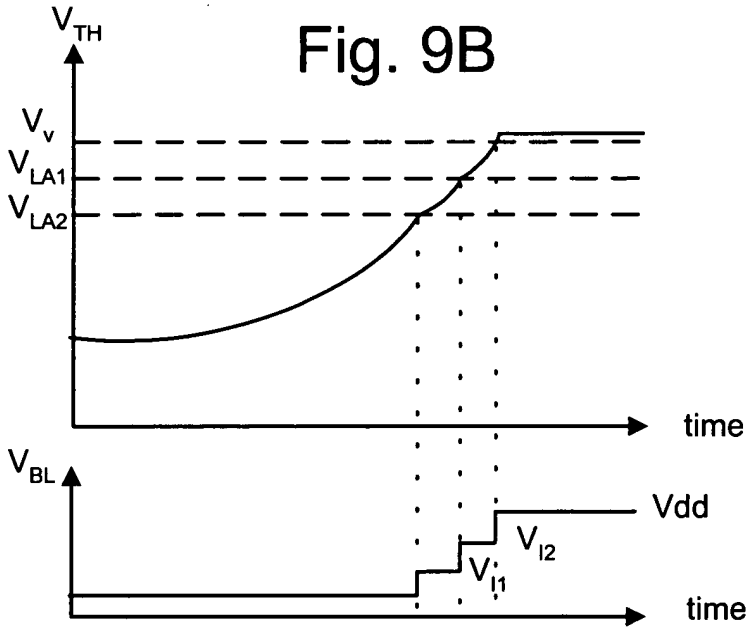

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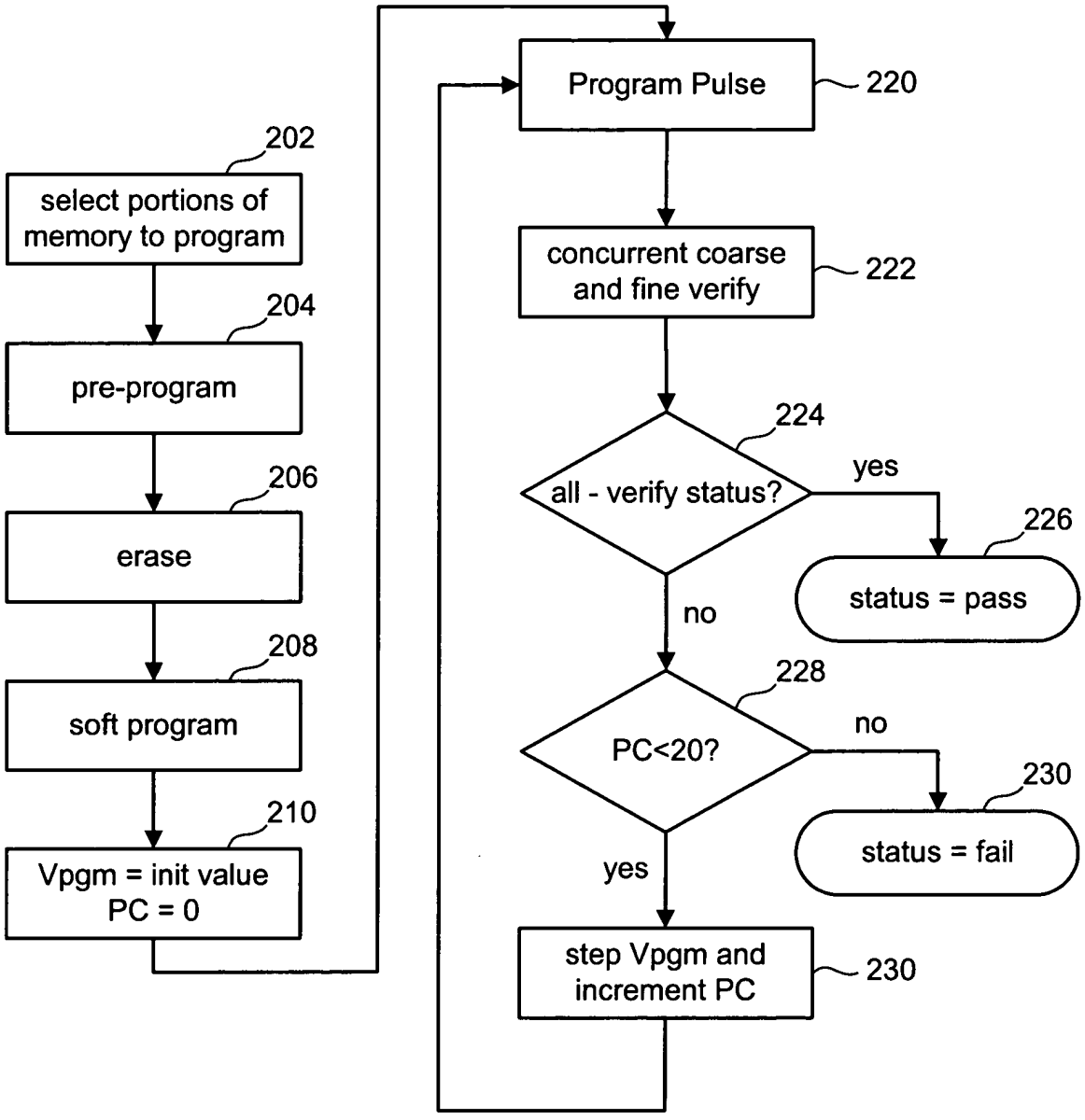
Fig. 10



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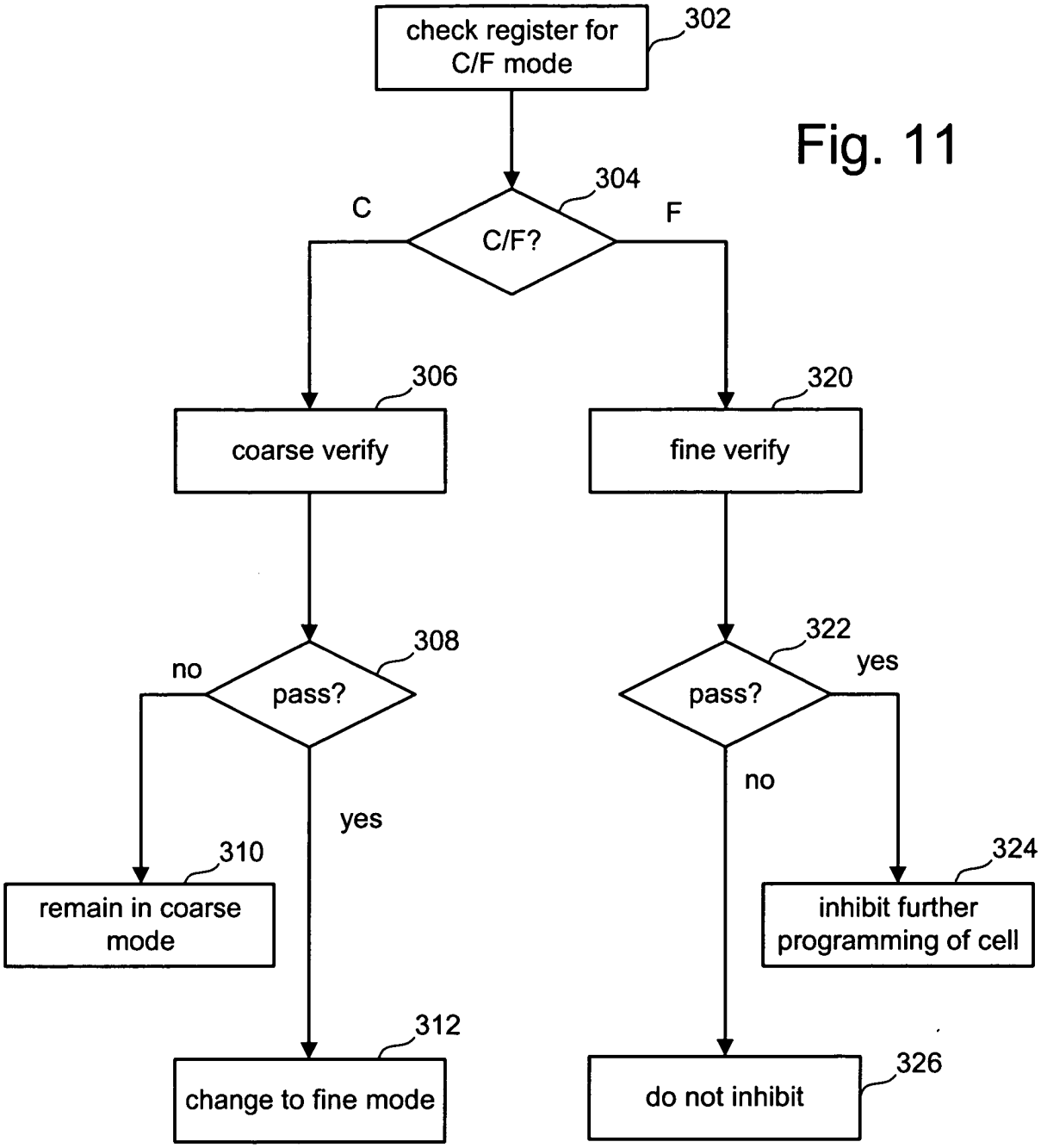

Fig. 11

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Fig. 12

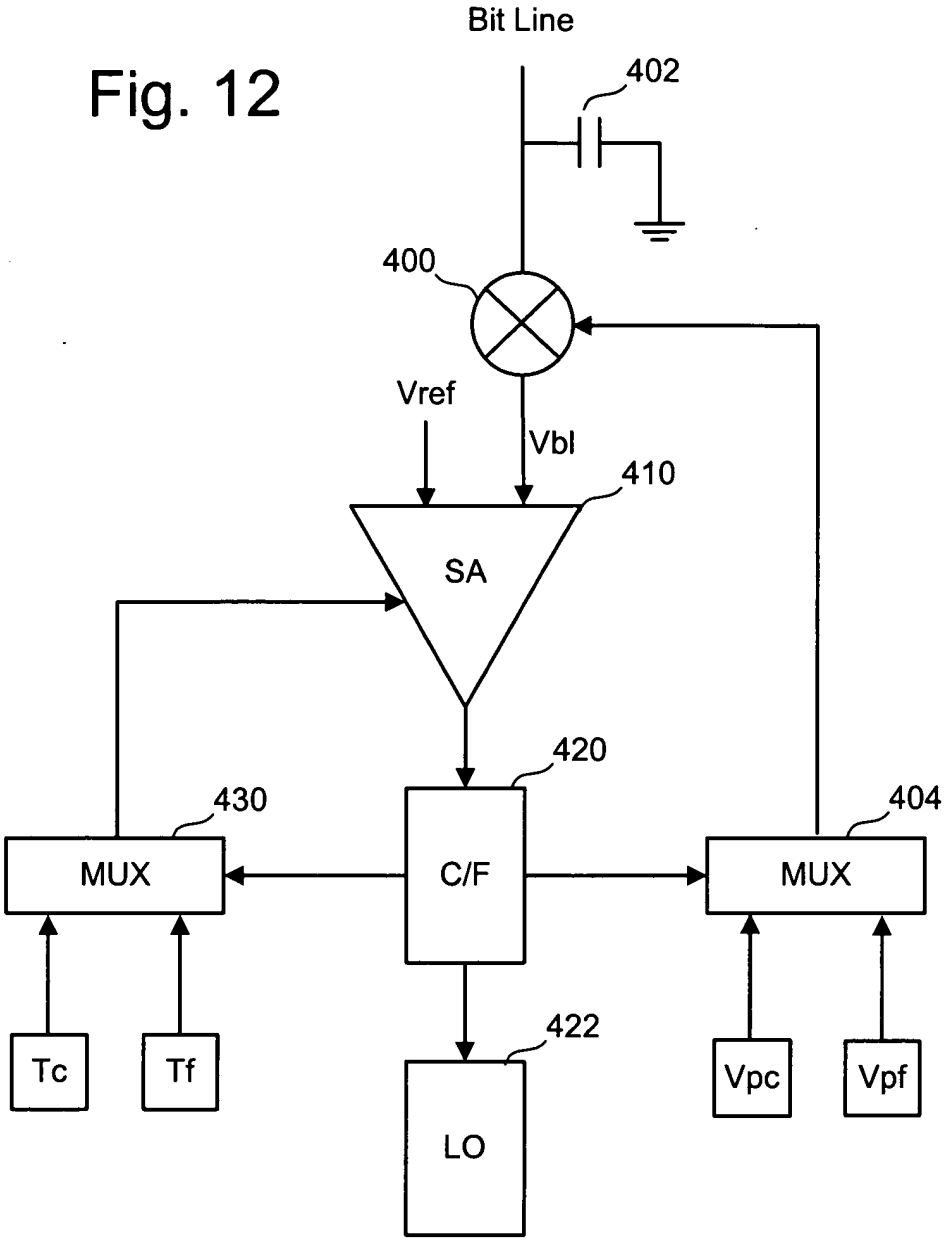

Fig. 13

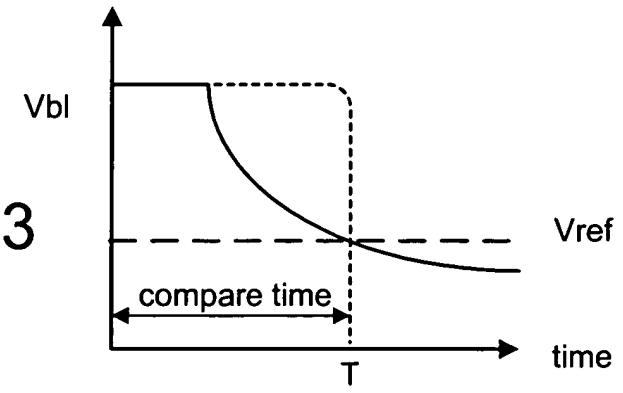

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Fig. 14

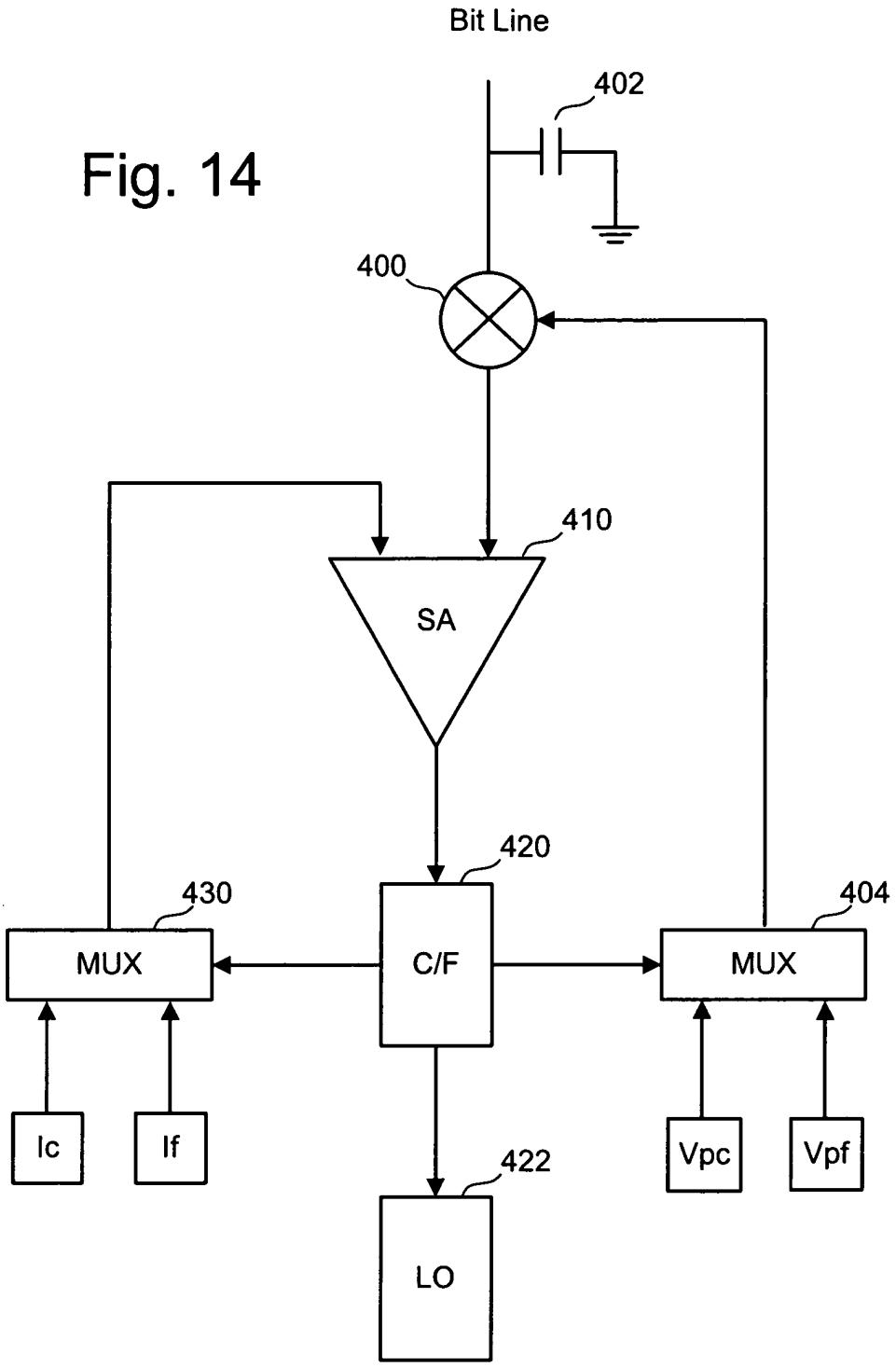

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Fig. 15

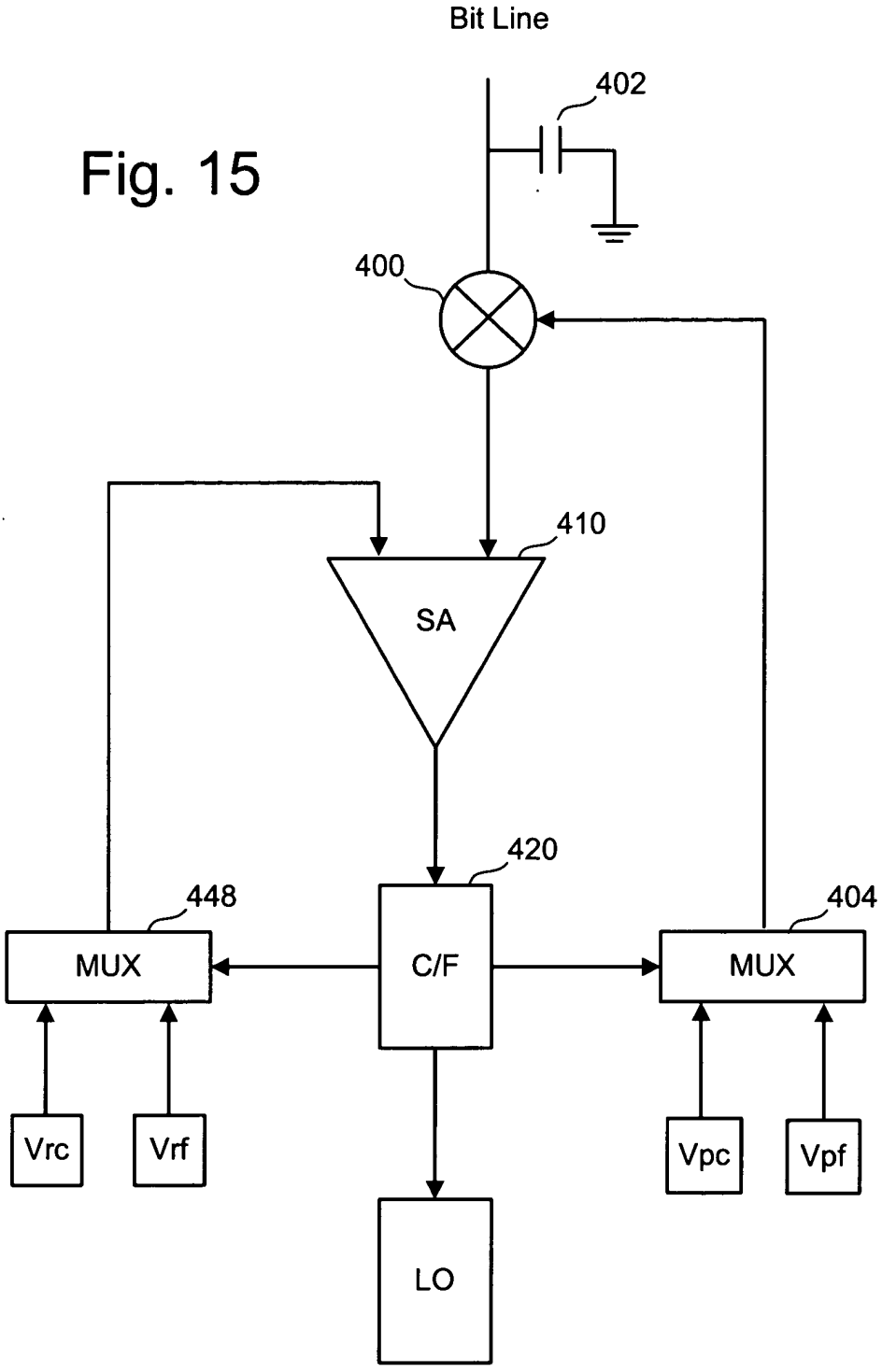

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Fig. 16

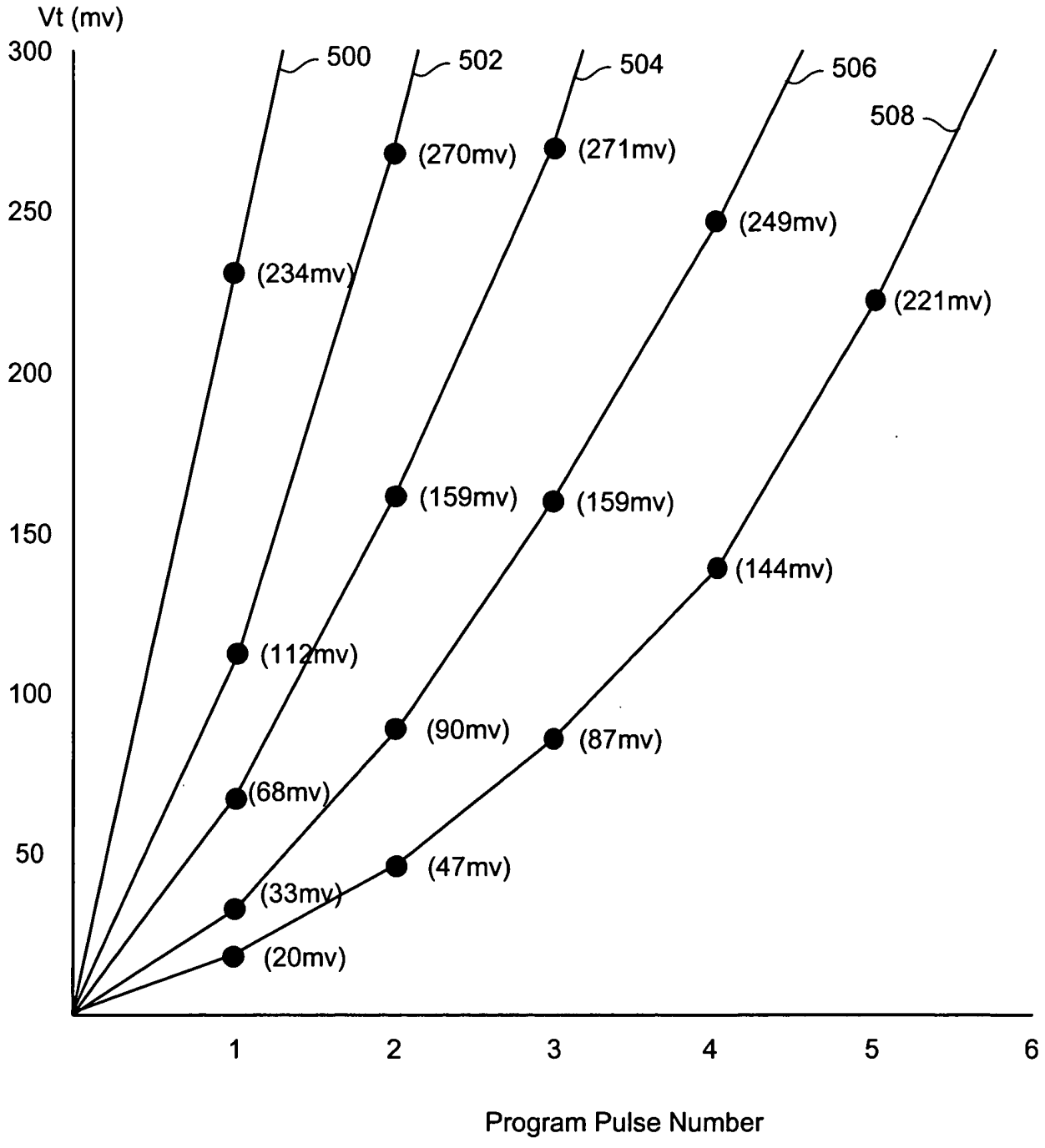

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Fig. 17

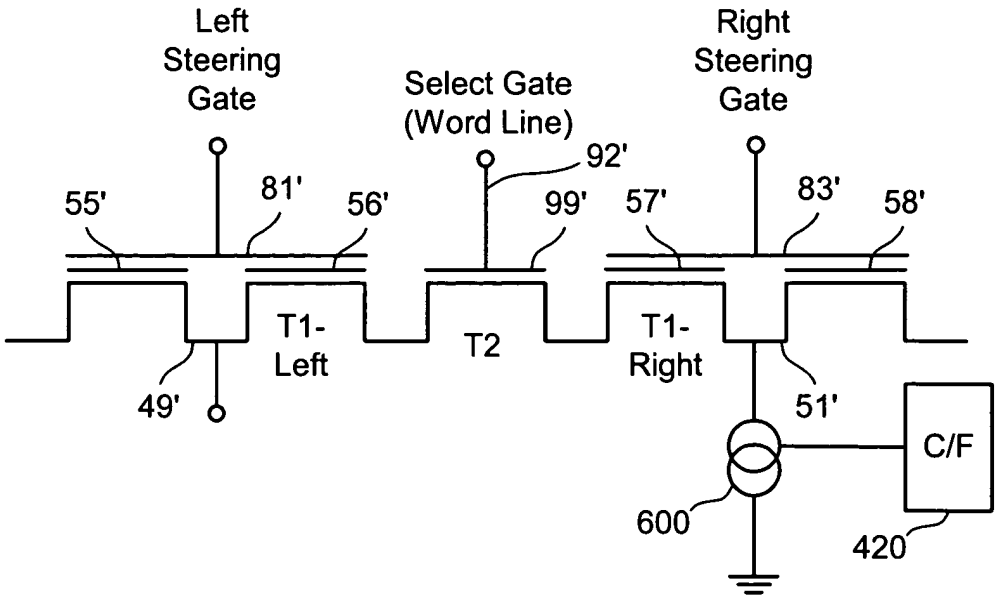

Fig. 18

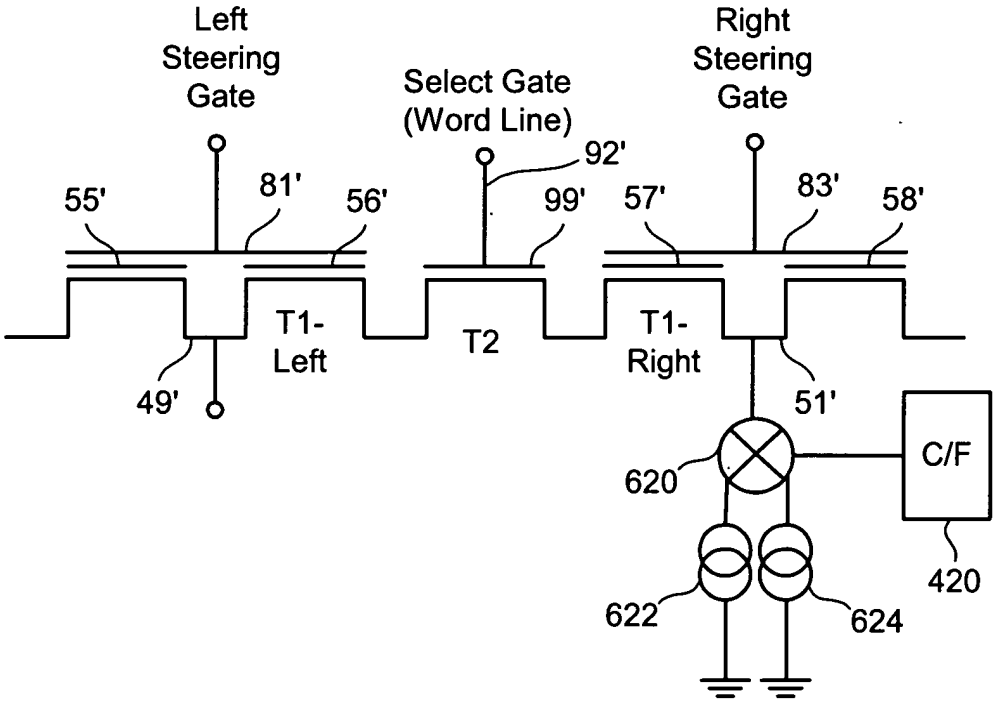

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Fig. 19

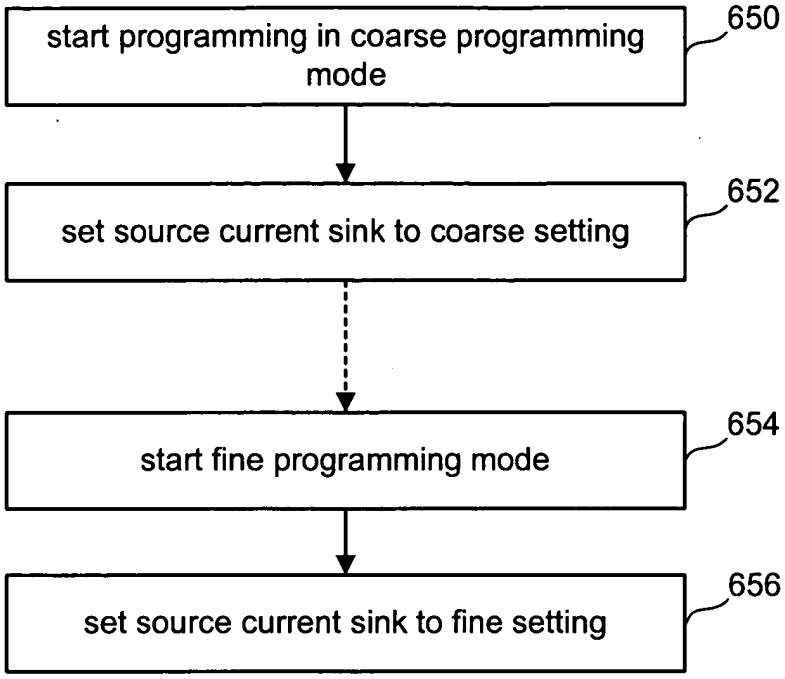
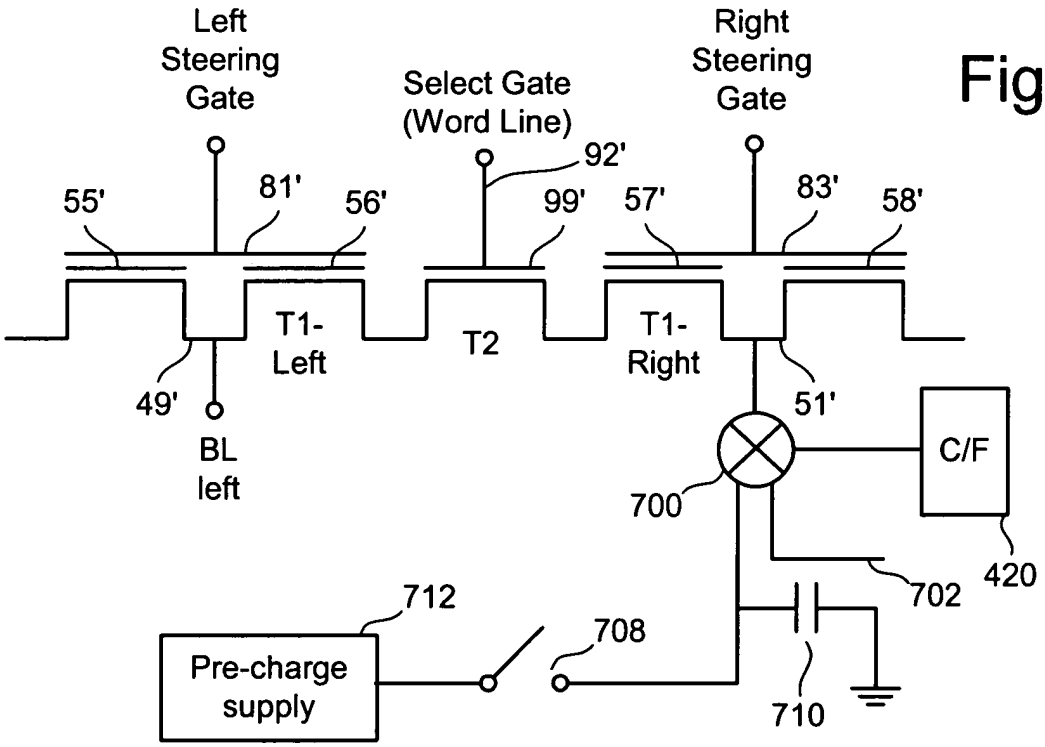


Fig. 20



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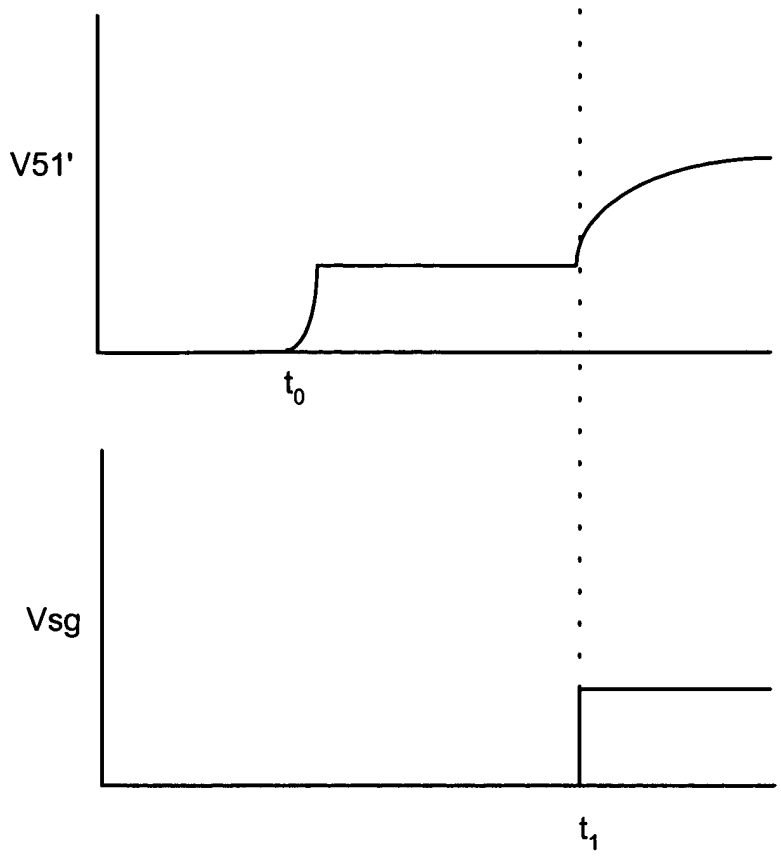

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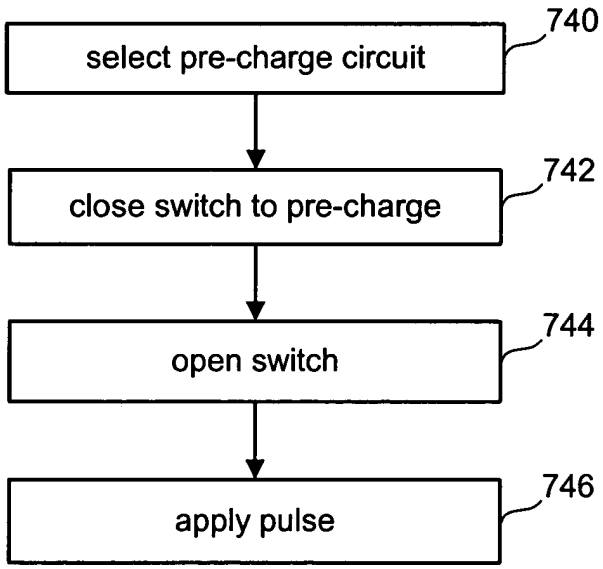

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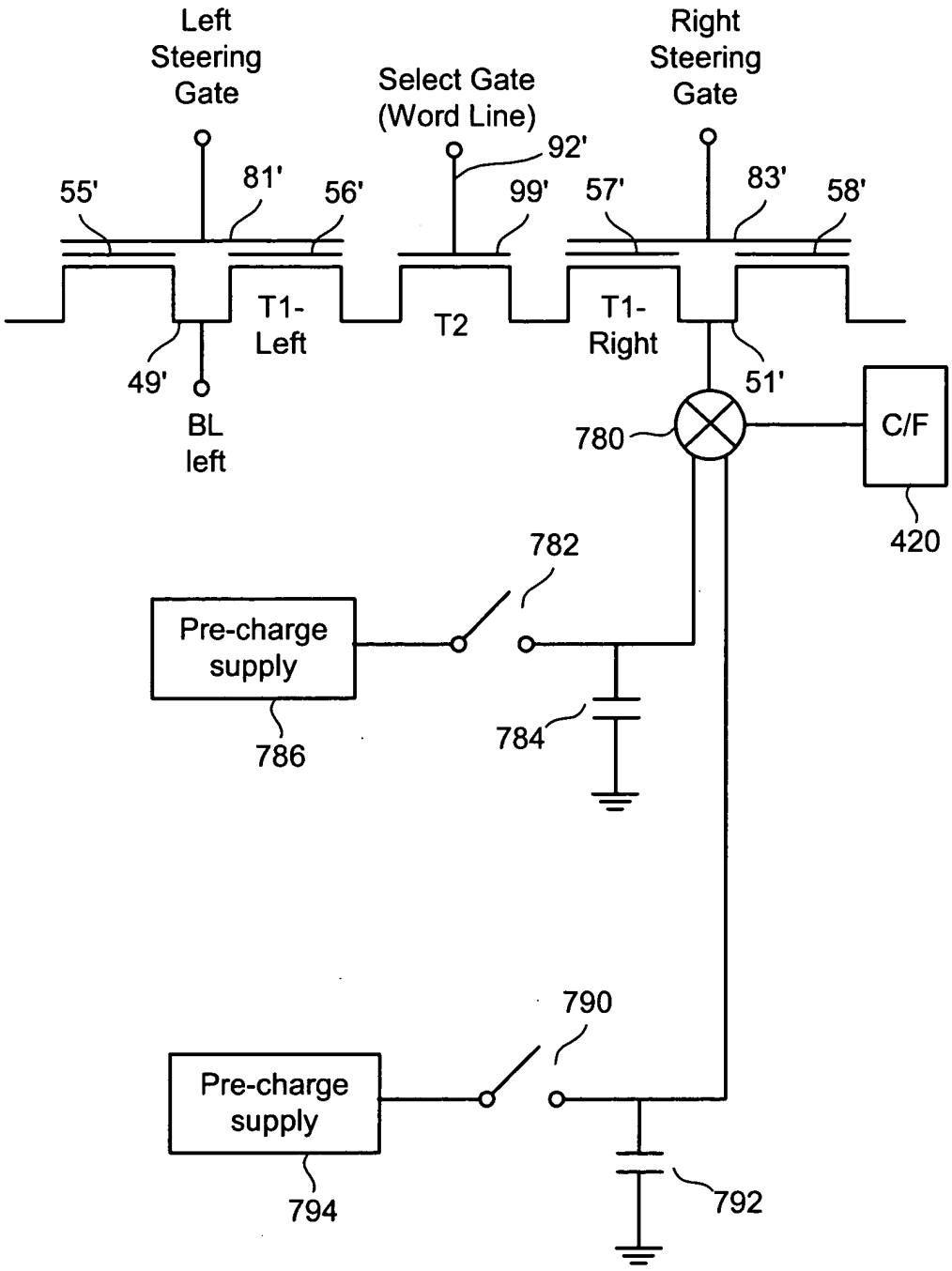

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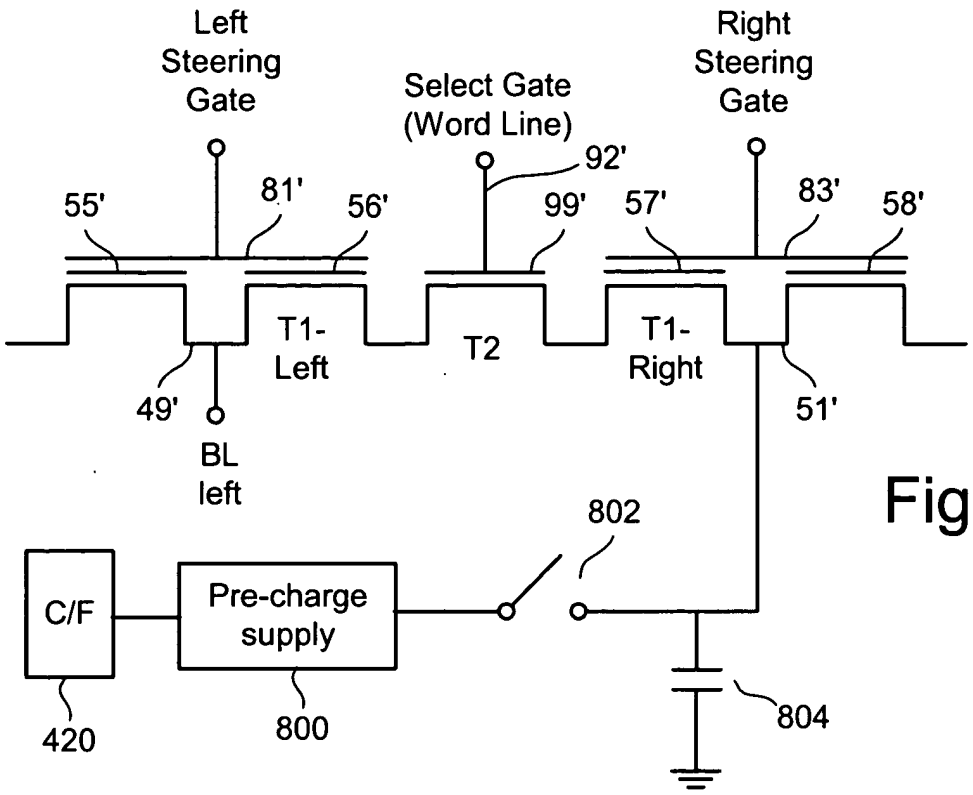

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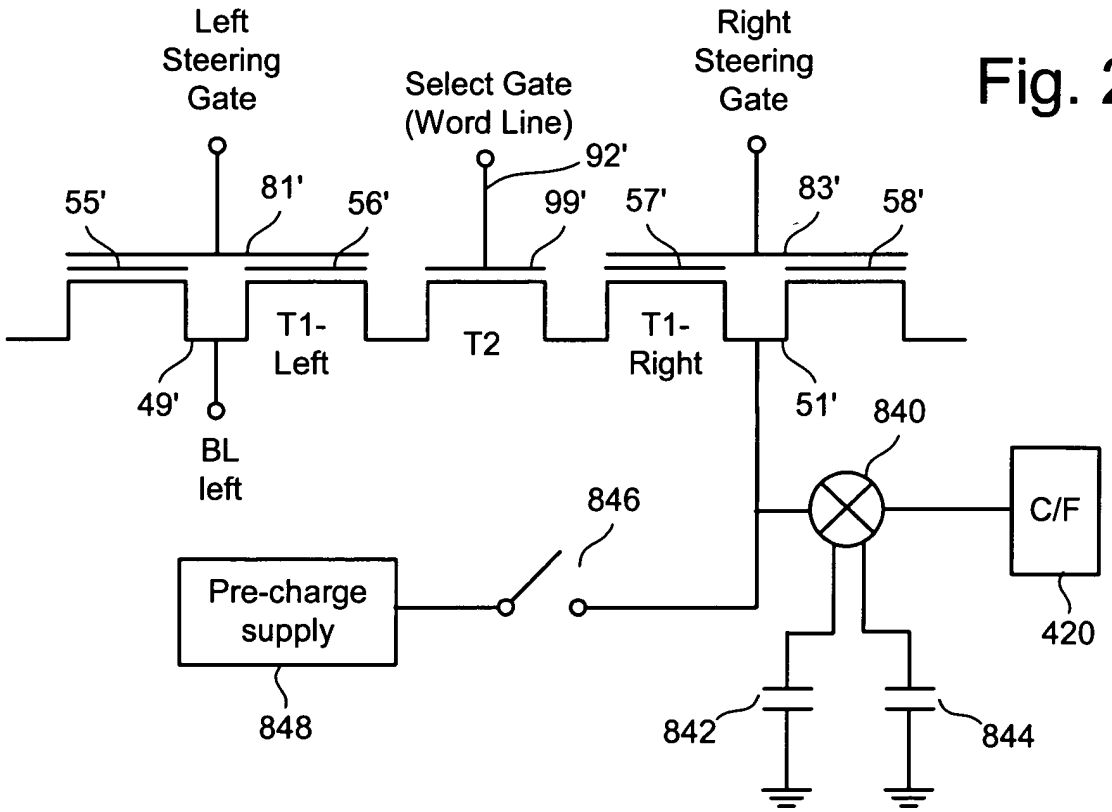

Fig. 25